NEX-EISA
EISA Bus Support Users Manual

Including these Software Support packages:
EISA

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TABLE OF CONTENTS

1.0 OVERVIEW 5
1.1 General Information 5
2.0 SOFTWARE INSTALLATION 5
2.1 TLA600/700 5
2.2 DAS9200 6
3.0 CONFIGURING the NEX-EISA BUS ADAPTER 6
3.1 General Information 6
3.2 Configuring for Slot Specific Signals 6
4.0 CONNECTING to the NEX-EISA ADAPTER 7
4.1 General 7
4.2 TLA600/700 7
4.3 92A96 7
5.0 CLOCK SELECTION 9
5.1 General Information 9
5.2 Clocking Options - Explanation 9
6.0 VIEWING DATA 9
6.1 Viewing State Data on the TLA600/700 9
6.2 Viewing Timing Data on the TLA600/700 12
6.3 Viewing State Data on the DAS9200/TLA500 13
6.4 Viewing Timing Data on the DAS9200/TLA500 13
APPENDIX A - Necessary Signals for Clocking 14
APPENDIX B - Considerations 15
B.1 EISA Loading 15
B.2 "Patch" Areas 15
B.3 Pattern Generation 15
B.4 Bus Masters 16
APPENDIX C - Modifying the NEX-EISA Support 17
APPENDIX D - EISA Bus Pinout 18
APPENDIX E - NEX-EISA Silk Screen 19
APPENDIX F - Support 20
APPENDIX G - References 21

TABLE OF FIGURES

Figure 1- EISA State Display on TLA600/700 10
Figure 2- EISA MagniVu Display on TLA600/700 12

TABLE OF TABLES

Table 1- EISA TLA600/700/92A96 Wiring 8
Table 2- EISA_Byte Bus Width Symbol Table 11
Table 3- EISA_I-O I/O Control Symbol Table 11

1.0 OVERVIEW

1.1 General Information

The NEX-EISA adapter has been designed to provide quick and easy connections to interface a 102- or 136-channel TLA600/700, a 92A96, or a 92C96 acquisition module to an EISA backplane. (The EISA designation refers to the Extended Industry Standard Architecture specification, an enhancement to the IBM PC XT/AT bus.) In addition, the method of connection permits the use of other acquisition cards, pattern generation cards or other measurement devices such as oscilloscopes.

The included software will permit the acquisition of EISA bus cycles, ignoring Idle and Wait states, and will display the data in easy-to-read symbolic form rather than raw hexadecimal or binary data.

Please note that this manual uses some terms generically. For instance, references to a 92A96 acquisition card apply to a 92C96 acquisition card; references to the DAS9200 apply equally to the TLA500; and references to the TLA700 apply to TLA600 and a TLA704, TLA711, 714, 715, 720 or 721 chassis with one or more 7*3/4 acquisition cards.

Appendix E is a silk-screen print of the NEX-EISA Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the EISA Bus specification and the Tektronix TLA600/700, DAS9200, or TLA500 Logic Analyzer. Also, in the case of the TLA600/700, it is expected that the user is familiar with Windows O.S.

For information on using a Prism 32GPX/GPD module with this support, or if 5¼" DAS floppies are needed, please contact Nexus Technology. See Appendix F for contact information.

2.0 SOFTWARE INSTALLATION

One 3½” diskette has been included with the NEX-EISA Bus Adapter. It is for use with the TLA600/700 series. Diskettes for the DAS9200 or TLA500 are available upon request. Please see Appendix E for contact information.

2.1 TLA600/700

The EISA support software is loaded in the same method as other Win95 programs. Place the NEX-EISA Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run

Add/Remove Programs, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose EISA and click on **Okay**. Note that for either support the Logic Analyzer card must be at least 102-channels in width.

2.2 DAS9200

The included diskette should be loaded onto the DAS9200 using the Install Application function. This function is available from the Disk Services menu of the DAS. For more information, refer to the Tektronix DAS9200 or TLA500 System User's Manual.

Load the desired support from within the 92A96 Config menu by choosing "EISA Support" and pressing <RETURN>. The channel grouping, clocking and symbols will then be loaded.

3.0 CONFIGURING the NEX-EISA BUS ADAPTER

3.1 General Information

The number of signals defined by the EISA specification exceeds the channel count of either a single 92A96 or a 102-channel TLA600/700 acquisition card. Because of this, jumper blocks have been created to permit the selective monitoring of specific signals. By placing a shorting jumper across the pair of pins next to the desired signal name, that signals can then be monitored during the acquisition. These jumper blocks are provided for the DAK~ (JP1), DRQ (JP2), and IRQ (JP3) signals. For information on physically modifying the NEX-EISA support to monitor the signals not provided by the standard implementation, refer to Appendix C.

3.2 Configuring for Slot Specific Signals

Another jumper block (JP5) has been provided to enable monitoring slot specific signals. These signals are MAK~, MREQ~, and AEN. To acquire these signals, connect the included flying leads to the appropriate signal pin, attach a grabber tip to the other end of the wire, then connect the grabber tip to a point on the backplane or target board to acquire these signals. It may be necessary to refer to schematics of the target board to determine where the signals can be probed. For reference, the signals may be acquired on the backplane at the following pins:

MAK~	H19
MREQ~	G19
AEN	A11

4.0 CONNECTING to the NEX-EISA ADAPTER

4.1 General

Although taller than a standard EISA module, the NEX-EISA adapter is designed to plug directly into any full-size EISA backplane slot. The board length and connector spacing conforms to EISA specifications.

4.2 TLA600/700

When using NEX-EISA support with a TLA600/700 containing a 7*3/4 acquisition module, the necessary acquisition data sections are A0-A3, D0-D3, and C0-C3. These grouped channels (8 podlets to a group) should be connected to the locations denoted for the A96. Follow the silk-screened information on the board that shows the proper relationship between the signal and reference inputs. When properly connected, the sides of the podlets that have writing on them should be visible.

Connect the four clock leads to their specified locations at J5 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the TLA600/700 when used with the NEX-EISA adapter.

4.3 92A96

When using a 92A96 or 92C96, connect the grouped pods to their appropriate locations by following the silk-screen information printed on the adapter board. The 92A/C96 pods are labeled A0-A3, D0-D3, and C0-C3. Each pod has its proper location denoted on the silk-screen of the adapter board. When attaching the pods, follow the silk-screen information on the board showing the ground and signal pin locations. When properly connected, the colored sides of the podlets should be visible.

Connect the four clock leads (one per A96 cable) to their specified locations at J5 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the 92A96 when used with the NEX-EISA adapter.

Group Name	Signal Name	EISA Pin #	TLA700 / 92A96 input	Group Name	Signal Name	EISA Pin #	TLA700 / 92A96 input
Address	LA23	C2	A3:7	Data	D31	G18	D3:7
(Hex)	LA22	C3	A3:6	(Hex)	D30	G17	D3:6
	LA21	C4	A3:5		D29	H16	D3:5
	LA20	C5	A3:4		D28	G14	D3:4
	LA19	C6	A3:3		D27	H14	D3:3
	LA18	C7	A3:2		D26	G13	D3:2
	LA17	C8	A3:1		D25	G12	D3:1
	LA16	F26	A3:0		D24	H12	D3:0
	LA15	E26	A2:7		D23	H11	D2:7
	LA14	F27	A2:6		D22	G10	D2:6
	LA13	E27	A2:5		D21	H10	D2:5
	LA12	E28	A2:4		D20	G9	D2:4
	LA11	E29	A2:3		D19	G8	D2:3
	LA10	F31	A2:2		D18	H8	D2:2
	LA9	E31	A2:1		D17	G7	D2:1
	LA8	H1	A2:0		D16	H7	D2:0
	LA7	G1	A1:7		D15	C18	D1:7
	LA6	H2	A1:6		D14	C17	D1:6
	LA5	H3	A1:5		D13	C16	D1:5
	LA4	G3	A1:4		D12	C15	D1:4
	LA3	G4	A1:3		D11	C14	D1:3
	LA2	H5	A1:2		D10	C13	D1:2
	SA1	A30	A1:1		D9	C12	D1:1
	SA0	A31	A1:0		D8	C11	D1:0
CycType	BALE	B28	C1:2		D7	A2	D0:7
(Hex)	MSBRST~	E9	C3:2		D6	A3	D0:6
	SLBRST~	E8	C3:1		D5	A4	D0:5
	BCLK	B20	C3:0		D4	A5	D0:4
	EXRDY	E3	C2:3		D3	A6	D0:3
	NOWS~	B8	C2:2		D2	A7	D0:2
	START~	E2	C2:1		D1	A8	D0:1
	ISAWR	*	C3:3		D0	A9	D0:0
BusWdth	BE3~	F15	C3:7	BusCtrl	IO16~	F10	A3:1
(Sym)	BE2~	F17	C3:6	(Bin)	EX32~	E4	C1:2
	BE1~	E17	C3:5		EX16~	E7	C1:1
	BE0~	F18	C3:4		M16~	D1	C1:0
I/O_Ctl	M-IO~	F10	A3:0		RFRSH~	B19	C0:1
(Sym)	W-R~	E10	C1:3		MSTR16~	D17	C0:0
	MRDC~	C9	C0:7	Misc	IRQX	---	A3:2
	MWTC~	C10	C0:6	(Bin)	DRQX	---	A3:3
	SMWTC~	B11	C0:5		DAKX~	---	A3:4
	SMRDC~	B12	C0:4		AENX	---	A3:5
	IOWC~	B13	C0:3		MREQX~	---	A3:6
	IORC~	B14	C0:2		MAKX~	---	A3:7
Cmd/Lok	CMD~	E1	C1:6		CHRDY	A10	C2:4
(Off)	LOCK~	F11	C1:5		IOCHK~	A1	C2:5
Clock:0	BCLK=	B20	- - - - -		T-C	B27	C1:7
Clock:1	ISAWR=	*	- - - - -		RESDRV	B2	C2:6
Clock:2	SLBRST~=	E8	- - - - -	Unused	C2:7	---	C2:7
Clock:3	MSBRST=	E9	- - - - -	(Off)			

Table 1- EISA TLA600/700/92A96 Wiring

* Derived signal

5.0 CLOCK SELECTION

5.1 General Information

There are two clocking options available when using the NEX-EISA support package. Each is explained in detail below.

When using a TLA600/700, the clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

When using a DAS9200 or TLA500, the clocking selection is made in the Clock menu.

5.2 Clocking Options - Explanation

Cycle Acquisition Only - This is the default clocking selection. In this mode every bus transaction is acquired. All Wait states are ignored. This clocking selection offers the best use of your acquisition memory by ignoring all Wait states, and also provides more easily understood data. Refer to Appendix A for a list of the signals necessary for this acquisition mode to work properly.

Acquire Every BCLK Edge - In this mode, data will be acquired on every edge of the EISA BCLK signal. This clocking mode shows *all* bus cycles, including Wait states. Since no clocking qualification is done only the BCLK signal is required.

6.0 VIEWING DATA

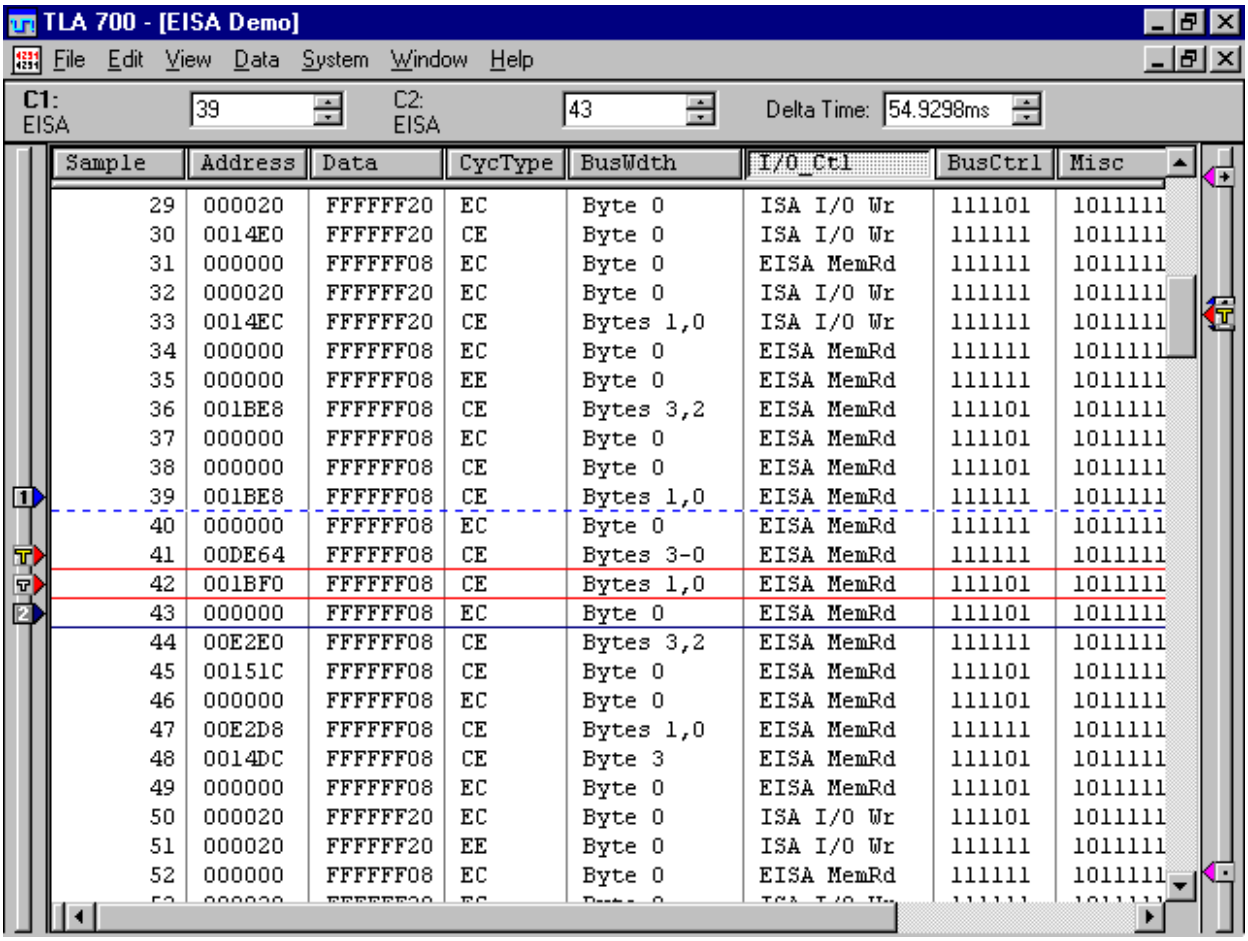
6.1 Viewing State Data on the TLA600/700

After making an initial acquisition, the TLA600/700 will display the data in the Listing (State) format. Address, Data, and Cycle Type (CycType) information is displayed in hexadecimal format; Bus Width (BusWdth) and I/O Control (I/O_Ctl) data is displayed using symbols; Bus Control (BusCtrl) and Miscellaneous (Misc) in binary, and the Command / Lock (Cmd/Lok) group is OFF.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. When using NEX-EISA, a symbol table (EISA_Byte, Table 2) has been provided for use with the BusWdth group to show what data bytes were valid during the transaction.

A second symbol table for the I/O_Ctl group (EISA_I-O, Table 3) shows whether the bus transaction was an EISA or ISA memory operation, an I/O operation, etc.

It is important to note that changing the group, channel, or wiring of the BusWdth or I/O_Ctl groups can result in incorrect symbol information being displayed.



Sample	Address	Data	CycType	BusWdth	I/O_Ctl	BusCtrl	Misc
29	000020	FFFFFF20	EC	Byte 0	ISA I/O Wr	111101	1011111
30	0014E0	FFFFFF20	CE	Byte 0	ISA I/O Wr	111111	1011111
31	000000	FFFFFF08	EC	Byte 0	EISA MemRd	111111	1011111
32	000020	FFFFFF20	EC	Byte 0	ISA I/O Wr	111111	1011111
33	0014EC	FFFFFF20	CE	Bytes 1,0	ISA I/O Wr	111111	1011111
34	000000	FFFFFF08	EC	Byte 0	EISA MemRd	111111	1011111
35	000000	FFFFFF08	EE	Byte 0	EISA MemRd	111111	1011111
36	001BE8	FFFFFF08	CE	Bytes 3,2	EISA MemRd	111101	1011111
37	000000	FFFFFF08	EC	Byte 0	EISA MemRd	111101	1011111
38	000000	FFFFFF08	CE	Byte 0	EISA MemRd	111101	1011111
39	001BE8	FFFFFF08	CE	Bytes 1,0	EISA MemRd	111111	1011111
40	000000	FFFFFF08	EC	Byte 0	EISA MemRd	111111	1011111
41	00DE64	FFFFFF08	CE	Bytes 3-0	EISA MemRd	111111	1011111
42	001BF0	FFFFFF08	CE	Bytes 1,0	EISA MemRd	111101	1011111
43	000000	FFFFFF08	EC	Byte 0	EISA MemRd	111101	1011111
44	00E2E0	FFFFFF08	CE	Bytes 3,2	EISA MemRd	111111	1011111
45	00151C	FFFFFF08	CE	Byte 0	EISA MemRd	111101	1011111
46	000000	FFFFFF08	EC	Byte 0	EISA MemRd	111101	1011111
47	00E2D8	FFFFFF08	CE	Bytes 1,0	EISA MemRd	111111	1011111
48	0014DC	FFFFFF08	CE	Byte 3	EISA MemRd	111101	1011111
49	000000	FFFFFF08	EC	Byte 0	EISA MemRd	111101	1011111
50	000020	FFFFFF20	EC	Byte 0	ISA I/O Wr	111101	1011111
51	000020	FFFFFF20	EE	Byte 0	ISA I/O Wr	111111	1011111
52	000000	FFFFFF08	EC	Byte 0	EISA MemRd	111111	1011111

Figure 1- EISA State Display on TLA600/700

Pattern	TLA700 / 92A96 Symbol
000	BYTES_3-0
001	BYTES_3-1
0010	ILLEGAL
0011	BYTES_3,2
0100	ILLEGAL
0101	ILLEGAL
0110	ILLEGAL
0111	BYTE_3
1000	BYTES_2-0
1001	BYTES_2,1
1010	ILLEGAL
1011	BYTES_2
1100	BYTES_1,0
1101	BYTE_1
1110	BYTE_0
1111	ILLEGAL

Table 2- EISA_Byte Bus Width Symbol Table

Signals, from left to right (MSB to LSB): BE3~, BE2~, BE1~, BE0~

Pattern	TLA700 / 92A96 Symbol	Meaning
11111111	EISA_MEMWR	EISA Memory Write
10111111	EISA_MEMRD	EISA Memory Read
01111111	EISA_I/O_WR	EISA I/O Write
00111111	EISA_I/O_RD	EISA I/O Read
xxx0xxxx	ISA_MEMWR	ISA MWTC~ Memory Write
xxxx0xxx	ISA_SMEMWR	ISA SMWTC~ Memory Write
xx0xxxxx	ISA_MEMRD	ISA MRDC~ Memory Read
xxxxx0xx	ISA_SMEMRD	ISA SMRDC~ Memory Read
xxxxxx0x	ISA_I/O_WR	ISA I/O Write
xxxxxxx0	ISA_I/O_RD	ISA I/O Read

Table 3- EISA_I-O I/O Control Symbol Table

Signals, from left to right (MSB to LSB): M-IO~, W-R~, MRDC~, MWTC~, SMWTC~, SMRDC~, IOWC~, and IORC~

6.2 Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: EISA and EISA-MagniVu. The first (EISA) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Timing format. The second selection, EISA-MagniVu, will show all of the channels in 2GHz/8GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

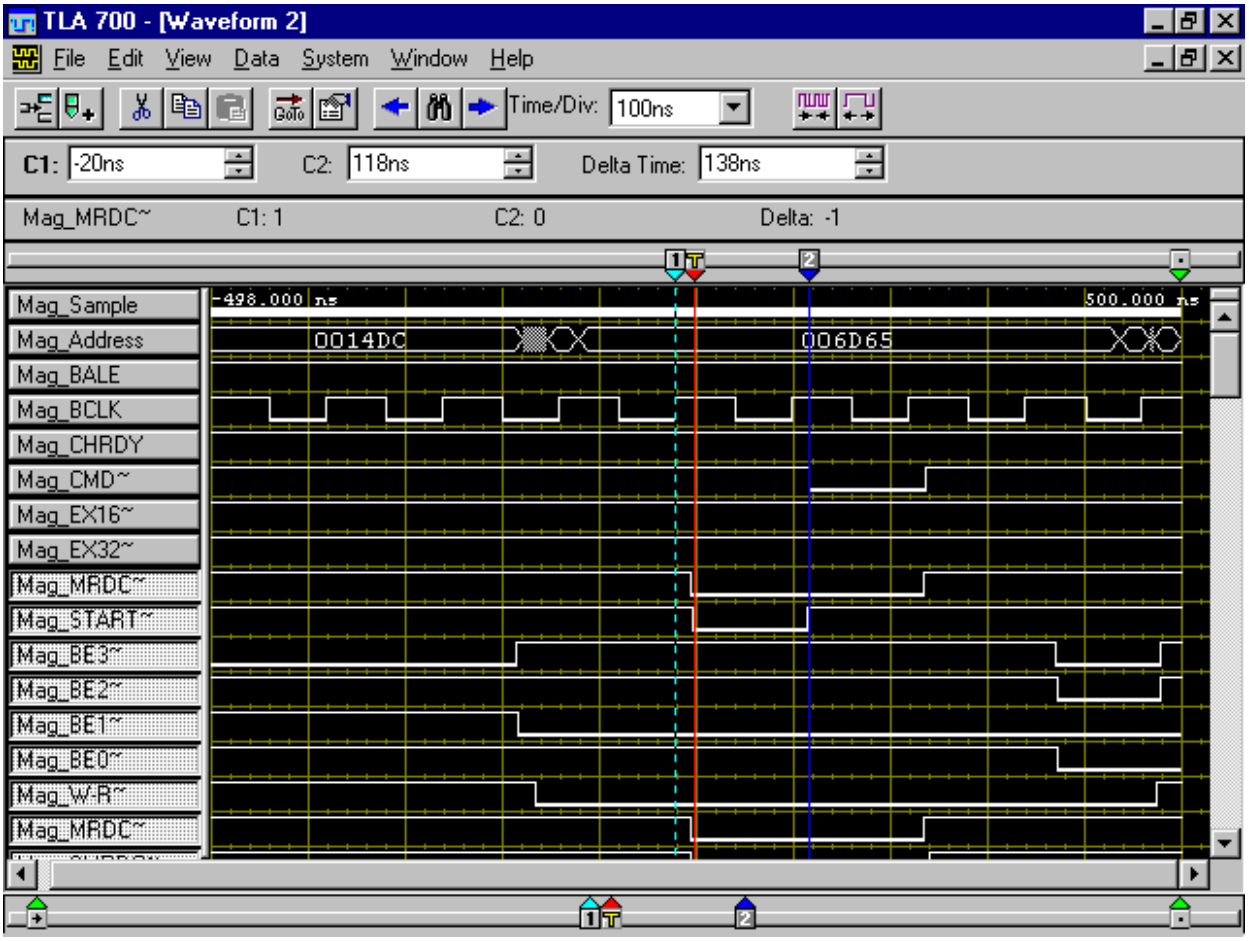


Figure 2- EISA MagniVu Display on TLA600/700

6.3 Viewing State Data on the DAS9200/TLA500

After an acquisition is made the DAS9200 Logic Analyzer will display the data in State Display mode (as a default only). Address, Data, and Cycle Type (CycType) information is displayed in hexadecimal format; Bus Width (BusWdth) and I/O Control (I/O_Ctl) data is displayed using symbols; Bus Control (BusCtrl) and Miscellaneous (Misc) in binary, and the Command / Lock (Cmd/Lok) group is OFF.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. When using NEX-EISA, a symbol table (EISA_Byte, Table 2) has been provided for use with the BusWdth group to show what data bytes were valid during the transaction.

A second symbol table for the I/O_Ctl group (EISA_I-O, Table 3) shows whether the bus transaction was an EISA or ISA memory operation, an I/O operation, etc.

It is important to note that changing the group, channel, or wiring of the BusWdth or I/O_Ctl groups can result in incorrect symbol information being displayed.

6.4 Viewing Timing Data on the DAS9200/TLA500

It may be useful to display acquired information using the Timing Diagram display of the DAS9200. (Note that, unlike some other logic analyzers, with the DAS9200 there is no need to re-acquire EISA data when changing from one display mode to another. The same data can be viewed in either format.) This method of data display can be particularly useful when an asynchronous acquisition has been made (using the DAS9200 internal acquisition clock) to determine the relationships between signal edges.

Refer to the appropriate Tektronix DAS 92A96 Module User's Manual for more detailed information on formatting the display of the acquired data.

APPENDIX A - Necessary Signals for Clocking

The 92A96 and 7*3/4 acquisition cards have very sophisticated internal clocking state machines. The NEX-EISA Support package software takes advantage of these functions to insulate the user from the chores of programming the acquisition card trigger program to acquire bus cycle data at the proper times.

When clocking data in “Cycle Acquisition Only” mode the following signals are necessary for proper acquisition of data: BCLK, SLBRST~, MSBRST~, BALE, START~, NOWS~, EXRDY, SMRDC~, SMWTC~, MWTC~, MRDC~, IORC~, and IOWC~.

When clocking data in “Acquire Every BCLK Edge” mode only the BCLK signal is necessary for data acquisition.

APPENDIX B - Considerations

B.1 EISA Loading

It must be noted that the NEX-EISA Bus Adapter does not provide any buffering of the EISA backplane signals, and violates the EISA specification of 2.5” maximum trace length. This was a conscious design decision that was made by balancing the tradeoffs of possible backplane loading versus signal acquisition accuracy. By not introducing signal buffers it is possible, using the NEX-EISA adapter, to see the exact timing relationships and signal waveforms from the backplane. It is also much easier to connect pattern generators to the backplane since buffer direction is not a concern. It is believed that the signal loading of the TLA600/700 or 92A96 acquisition cards is low enough so that EISA signal degradation will not occur.

The NEX-EISA Adapter Board was designed so that the run lengths for critical signals (and those with the highest activity levels, such as the address / data bus) are as short as possible. This should help greatly in retaining signal integrity.

B.2 "Patch" Areas

If signal loading or reflection does become a concern, the capability exists to add series resistors to any EISA signal. Patch areas have been provided next to each TLA600/700/A96 connector, consisting of two rows of plated through holes. These areas (outlined on the silk-screen and labeled as Nxx) are suitable for individual resistors or resistor networks. To add a series resistor, simply cut the trace of the desired signal on the component side of the board, and solder the resistor between the two feed-throughs.

B.3 Pattern Generation

Because there is no buffer circuitry on the NEX-EISA Adapter, it is well suited for use with the 92S16 and 92S32 Pattern Generator modules available for the DAS9200. By connecting pattern generator probes to the A96 signal connectors on the Adapter, desired bus activity can be simulated. This can be particularly effective when trying to debug interrupt or DMA conflicts.

It should be noted that, because of the pin spacing of the A96 connectors, it is not recommended that the Tektronix P6464 or P6465 pattern generator probes be used without providing adequate cooling for their podlets. These probes use active podlets that can get very warm in use. A better choice would be the P6463 pods which are passive and do not have such cooling requirements.

B.4 Bus Masters

Because of the pipelined nature of the EISA Burst cycles, the address and corresponding data information occur in different cycles. Since this information is acquired and logged at two different times (in two different bus cycles), it is not possible to realign the address with the correct data. The very first Burst acquisition displayed will have invalid data associated with it as the data is valid one cycle later. The final Burst acquisition will have an invalid address value displayed, while the data is valid and associated with the previous acquisition.

APPENDIX C - Modifying the NEX-EISA Support

As previously mentioned, the EISA specification has too many signals to be acquired with one 92A96 or 102-channel TLA600/700 card. Assumptions have been made as to what signals are of interest, but these assumptions may not be appropriate in every instance. For these occasions, the NEX-EISA support may be easily modified to monitor any desired signals.

When using a 92A96 or TLA600/700 acquisition car dot monitor additional signals, the modification method is very simple. All EISA signals (including the Reserved and Undefined ones) have been brought out to 92A96/TLA600/700 compatible acquisition points (dual-row connectors). Take the A96/TLA600/700 pod that will be used to monitor these signals and move it to the desired signal group. If necessary, the group can be separated into 8 individual podlets to probe different acquisition groups.

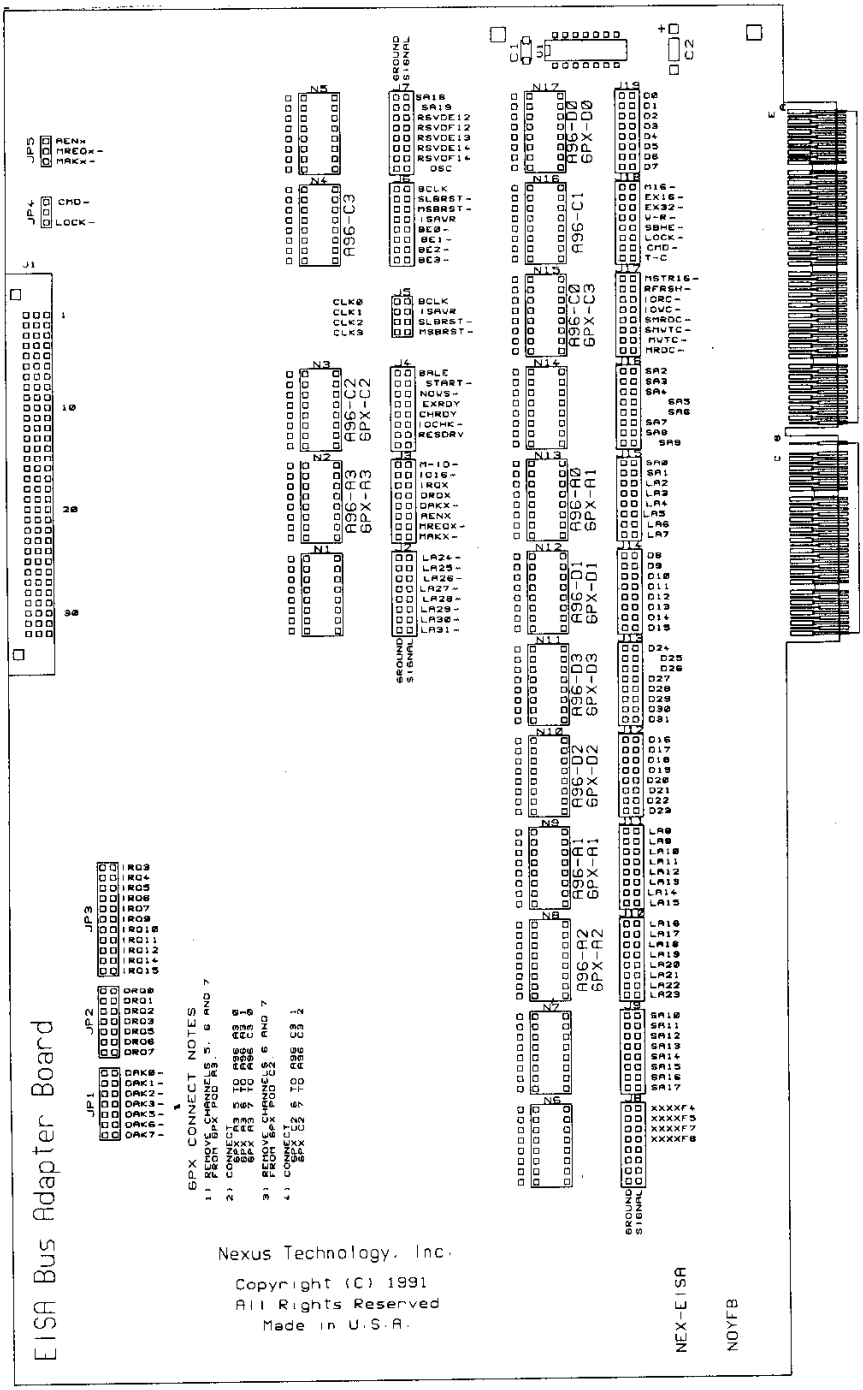
The channel grouping default for the NEX-EISA support will then have to be changed. Refer to the appropriate Logic Analyzer manual for information on how this can be done. Note that when changing any of the signals in the BusWdth or I/O_Ctl groups that their included Symbol Tables will no longer be accurate.

APPENDIX D - EISA Bus Pinout

Pin #	Row F - Solder Side	Row B - Solder Side	Row E - Component Side	Row A - Component Side
1	Ground	Ground	CMD~	-IOCHK
2	+5V	RESET	START~	SD7
3	+5V	+5V	EXRDY	SD6
4	XXXXXX	IRQ9	EX32~	SD5
5	XXXXXX	-5V	GND	SD4
6	<Key>	DRQ2	<Key>	SD3
7	XXXXXX	-12V	EX16~	SD2
8	XXXXXX	-0WS	SLBURST~	SD1
9	+12V	+12V	MSBURST~	SD0
10	M-IO~	Ground	W-R~	IORDY
11	LOCK~	-SMEMW	Ground	AEN
12	Reserved	-SMEMR	Reserved	SA19
13	Ground	-IOW	Reserved	SA18
14	Reserved	-IOR	Reserved	SA17
15	BE3~	-DAK3	Ground	SA16
16	<Key>	DRQ3	<Key>	SA15
17	BE2~	-DAK1	BE1~	SA14
18	BE0~	DRQ1	LA31~	SA13
19	Ground	REFRSH	Ground	SA12
20	+5V	CLK	LA30~	SA11
21	LA29~	IRQ7	LA28~	SA10
22	Ground	IRQ6	LA27~	SA9
23	LA26~	IRQ5	LA25~	SA8
24	LA24~	IRQ4	Ground	SA7
25	<Key>	IRQ3	<Key>	SA6
26	LA16	-DAK2	LA15	SA5
27	LA14	T/C	LA13	SA4
28	+5V	BALE	LA12	SA3
29	+5V	+5V	LA11	SA2
30	Ground	OSC	Ground	SA1
31	LA10	Ground	LA9	SA0

Pin #	Row H - Solder Side	Side D - Solder Side	Row G - Component Side	Side C - Component Side
1	LA8	-MEM16	LA7	SBHE
2	LA6	-IO16	Ground	LA23
3	LA5	IRQ10	LA4	LA22
4	+5V	IRQ11	LA3	LA21
5	LA2	IRQ12	Ground	LA20
6	<Key>	IRQ15	<Key>	LA19
7	D16	IRQ14	D17	LA18
8	D18	-DAK0	D19	LA17
9	Ground	DRQ0	D20	-MEMR
10	D21	-DAK5	D22	-MEMW
11	D23	DRQ5	Ground	SD8
12	D24	-DAK6	D25	SD9
13	Ground	DRQ6	D26	SD10
14	D27	-DAK7	D28	SD11
15	<Key>	DRQ7	<Key>	SD12
16	D29	+5V	Ground	SD13
17	+5V	-MASTER	D30	SD14
18	+5V	Ground	D31	SD15
19	MAKx~	- - - - -	MREQx~	- - - - -

APPENDIX E - NEX-EISA Silk Screen



APPENDIX F - Support

About Nexus Technology, Inc.

Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

Nexus Technology, Inc.
78 Northeastern Blvd. #2
Nashua, NH 03062

TEL: 877-595-8116
FAX: 877-595-8118

Web site: http://**www.nexustechnology.com**

Support Contact Information

Technical Support	**techsupport@nexustechnology.com**
General Information	**support@nexustechnology.com**
Quote Requests	**quotes@nexustechnology.com**

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX G - References

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Logic Analyzer User's Manual

Tektronix DAS9200 / TLA500 System User's Manual

Tektronix 92A96 / 92C96 Module User's Manual

"AT Bus Design" by Edward Solari
Published by Annabooks, San Diego, CA